DEVICE TECHNOLOGY

Aligned, high-density semiconducting carbon nanotube arrays for high-performance electronics

Lijun Liu[1]*, Jie Han[1]*, Lin Xu[1], Jianshuo Zhou[1], Chenyi Zhao[1], Sujuan Ding[2,3], Huiwen Shi[1], Mengmeng Xiao[1], Li Ding[1], Ze Ma[1], Chuanhong Jin[2,3], Zhiyong Zhang[1,2,4]†, Lian-Mao Peng[1,2,4]†

Single-walled carbon nanotubes (CNTs) may enable the fabrication of integrated circuits smaller than 10 nanometers, but this would require scalable production of dense and electronically pure semiconducting nanotube arrays on wafers. We developed a multiple dispersion and sorting process that resulted in extremely high semiconducting purity and a dimension-limited self-alignment (DLSA) procedure for preparing well-aligned CNT arrays (within alignment of 9 degrees) with a tunable density of 100 to 200 CNTs per micrometer on a 10-centimeter silicon wafer. Top-gate field-effect transistors (FETs) fabricated on the CNT array show better performance than that of commercial silicon metal oxide–semiconductor FETs with similar gate length, in particular an on-state current of 1.3 milliamperes per micrometer and a recorded transconductance of 0.9 millisiemens per micrometer for a power supply of 1 volt, while maintaining a low room-temperature subthreshold swing of <90 millivolts per decade using an ionic-liquid gate. Batch-fabricated top-gate five-stage ring oscillators exhibited a highest maximum oscillating frequency of >8 gigahertz.

The development of modern integrated circuits (ICs) has required scaling of field-effect transistors (FETs) to provide increased density, performance, and energy efficiency (*1*). Ultrathin semiconducting channels with high carrier mobility minimize the short-channel effect in aggressively scaled FETs (such as sub–10 nm technology nodes) (*2*). Single-walled carbon nanotubes (CNTs) can be 10 times as energy-efficient as conventional complementary metal oxide–semiconductor (CMOS) FETs because electron transport is ballistic, and CNTs have excellent electrostatic properties (*2*–*5*). Furthermore, prototype transistors built on individual CNTs with gate lengths as short as 5 nm outperform Si CMOS transistors in terms of both intrinsic performance and power consumption (*5*).

However, CNT FETs with real performance exceeding that of Si CMOS FETs have not been realized at similar technology nodes because CNT materials available for research are still far from ideal for electronics. As a building block for high-performance digital electronics, the extremely scaled CNT FET (with a channel width of several tens of nanometers; Fig. 1A) should contain multiple semiconducting CNTs in the channel to provide sufficient driving ability (*2*–*6*). A high-density aligned semiconducting CNT array is required as the channel material for fabricating large-scale ICs. The ideal material system is well established to be aligned CNT (A-CNT) arrays with a well-defined and consistent 5- to 10-nm pitch (100 to 200 CNTs/μm), a semiconducting purity estimated to be >99.9999%, and a narrow diameter distribution around 1.5 nm (Fig. 1B) (*3*).

Although A-CNTs have been produced through chemical vapor deposition (CVD) growth of nanotubes on quartz or sapphire with high density (up to 100 CNTs/μm) or high semiconducting purity obtained through post-treatment (up to 99.9999%) (*7*–*9*), arrays with both high density and high purity have not yet been demonstrated. As a result, FETs built on CVD-grown CNT arrays suffer from either a low current on/off ratio (because of low purity) or a low driving current (because of low density) (*2*, *3*). Also, each device based on CVD-grown CNT arrays contains an undefined number of nanotubes, also known as an inconsistent pitch, which contributes to large device-to-device variation (*2*, *10*, *11*).

"Purified-and-placed" solution-processed CNT materials can provide CNTs with high semiconducting purity. This approach is simple and scalable, and it could provide wafer-scale assembly capability (*12*–*18*), but challenges remain. The current level of semiconducting purity of 99.99% must be improved to 99.9999% by further sorting CNTs and upgrading the purity characterization method. The solution-derived CNTs must be aligned into arrays with a 5- to 10-nm consistent pitch and full wafer coverage (*2*, *3*, *5*, *18*, *19*). A variety of methods have been developed to assemble solution-processed CNTs into arrays on substrates (*20*–*25*).

Arnold and colleagues (*20*, *21*) reported a method to produce CNT arrays with a density of 47 CNTs/μm and built quasi-ballistic FETs with a high on-state current. However, the FETs thus fabricated suffered from low transconductance (0.1 mS/μm) because of low CNT density and poor gate efficiency, and the CNT arrays used had a strip-like shape that could not fully cover the substrate. Additionally, high-density and full-coverage CNT arrays have been prepared through methods such as the Langmuir-Schaefer–based method (*23*) or the vacuum filtration method (*26*). However, the CNT arrays thus obtained typically have a very high CNT array density of >400 CNTs/μm, resulting in a low on-state performance (in terms of transconductance g_m and on-state current I_{on} per tube) and a low current on/off ratio because of inefficient metal contacts with CNTs as well as serious screening effects from deleterious intertube interactions (*3*, *21*, *27*). To

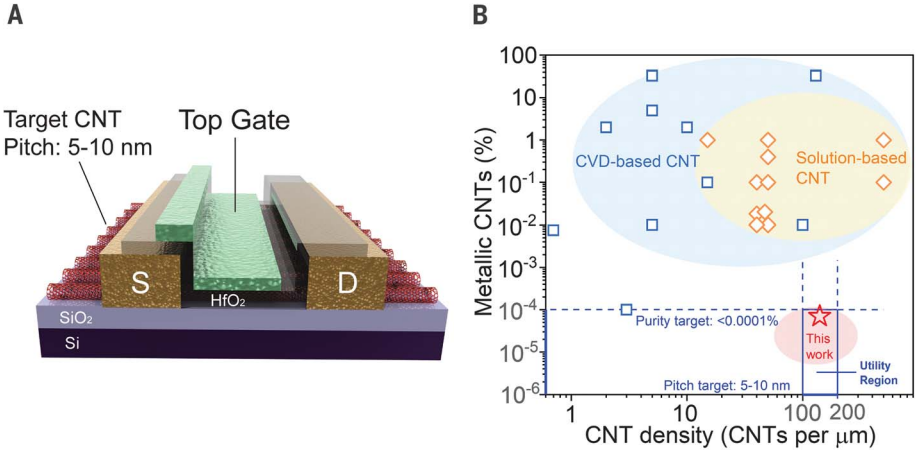

Fig. 1. Transistor structure and material target for CNT FET–based digital IC technology. (**A**) Schematic diagram showing a CNT-based top-gate FET with an ideal 5- to 10-nm CNT pitch. S, source; D, drain. (**B**) Semiconducting purity versus density of CNT arrays. The utility region is marked as a blue hollow box, and our results are located in the pink region, with a typical one marked as a red star. The extracted data (blue rectangles and orange diamonds) are listed in table S1 (*7*–*9*, *17*, *20*–*23*, *29*, *32*–*44*).

[1]Key Laboratory for the Physics and Chemistry of Nanodevices and Center for Carbon-based Electronics, Department of Electronics, Peking University, Beijing 100871, China. [2]Hunan Institute of Advanced Sensing and Information Technology, Xiangtan University, Hunan 411105, China. [3]State Key Laboratory of Silicon Materials, School of Materials Science and Engineering, Zhejiang University, Hangzhou, 310027, China. [4]Frontiers Science Center for Nano-optoelectronics, Peking University, Beijing 100871, China.
*These authors contributed equally to this work.
†Corresponding author. Email: zyzhang@pku.edu.cn (Z.Z.); lmpeng@pku.edu.cn (L.-M.P.)

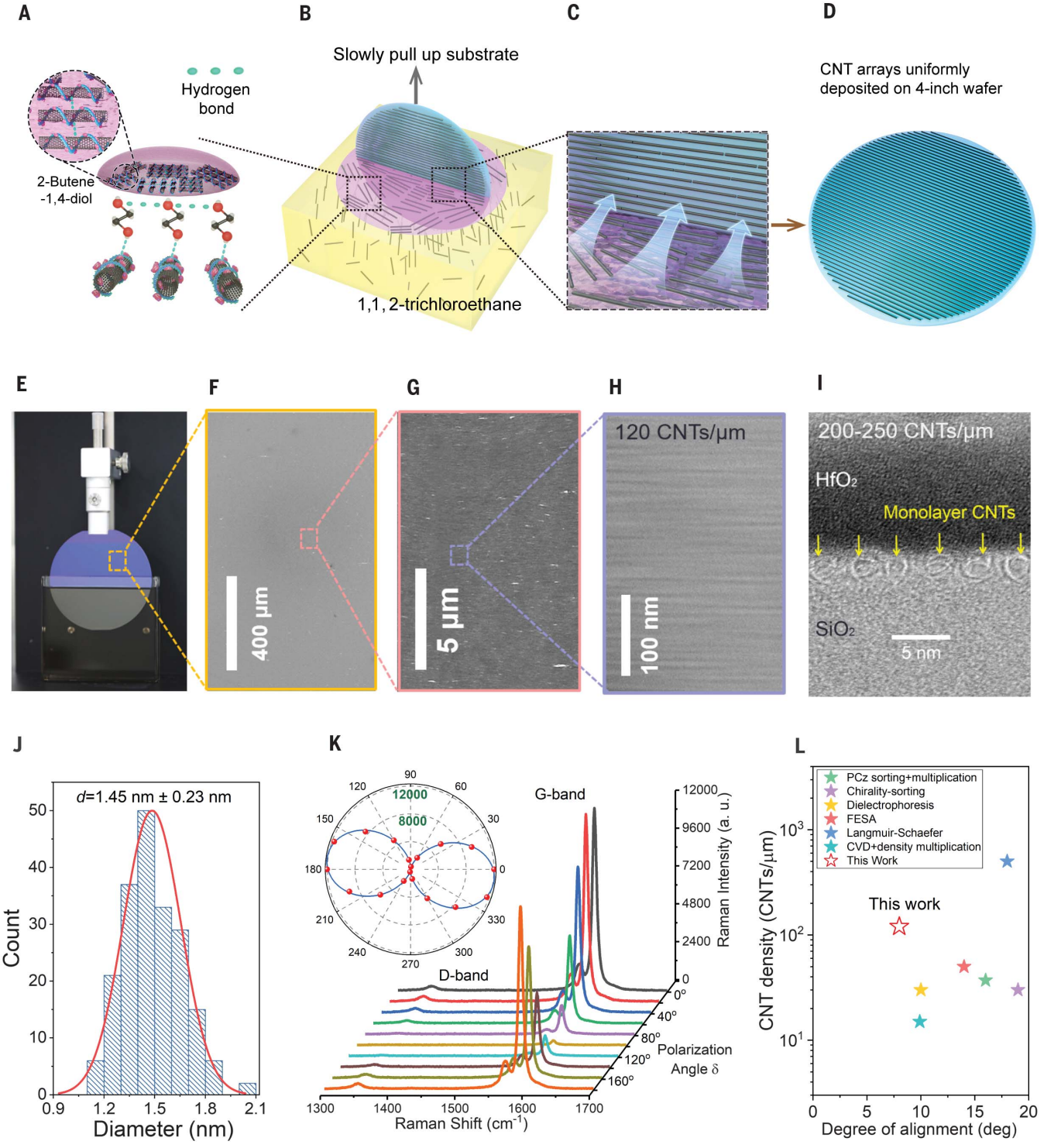

Fig. 2. Preparation and characterization of an A-CNT array. (**A** to **D**) Schematic images showing the process of preparing a wafer-scale A-CNT array. (**E**) Optical image showing the dip-coating setup used for coating CNTs on a 4-inch silicon wafer. (**F** to **H**) SEM images showing an as-deposited CNT array obtained using an optimal CNT solution concentration (40 μg/ml) at different magnifications. (**I**) Cross-section TEM image of a CNT array obtained using the highest CNT solution concentration of 60 μg/ml. The CNTs clearly show a density of at least 200 CNTs/μm (<5 nm pitch); even at this high CNT density, our CNT arrays still present a good monolayer property, which is crucial for electronics applications. (**J**) Diameter distribution of 200 CNTs measured by TEM. (**K**) Polarized Raman spectra of CNTs for different incident angles δ. The polarization angle of the incident light was changed through rotating a λ/2 wave plate during the measurements, and the reference (zero angle) is not exactly parallel to the CNT array. Inset: The Raman intensity is extracted and fitted in polar coordinates. (**L**) Benchmarking of the degree of alignment as a function of CNT density. All data used here are listed in table S2 (*9*, *20*, *23*, *25*, *49*, *50*).

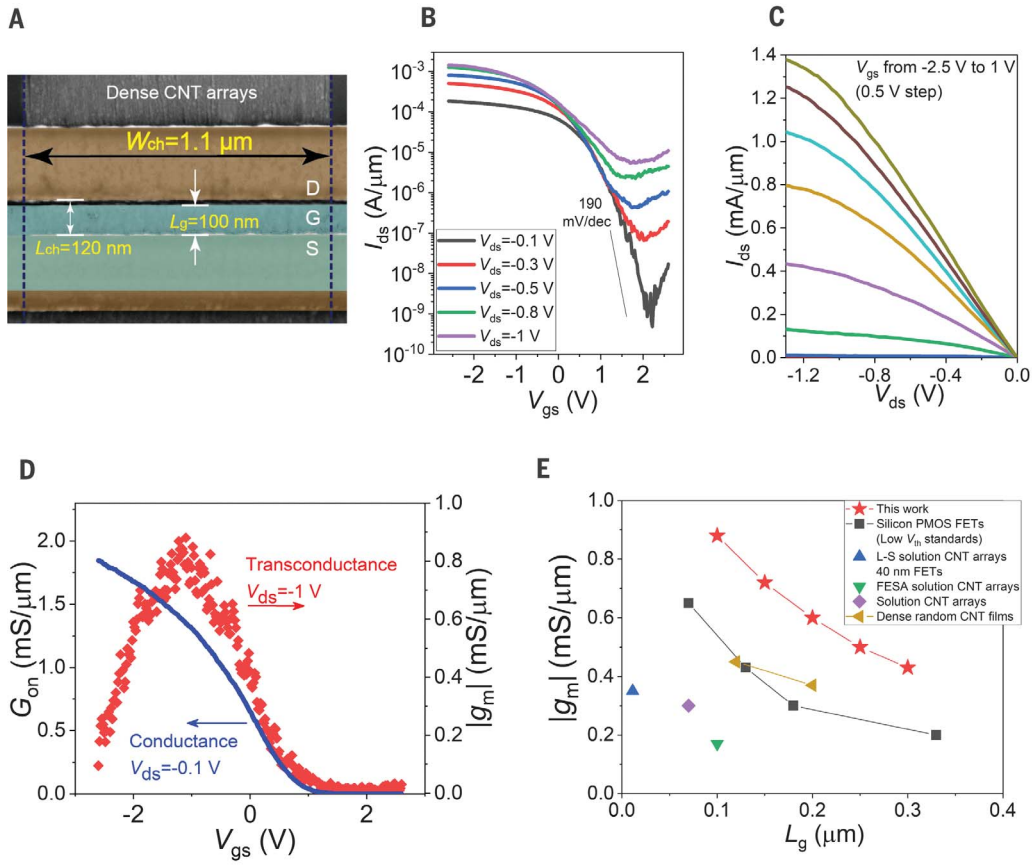

Fig. 3. Characteristics and benchmarking of A-CNT array–based top-gate FETs. (**A**) SEM image with a detailed channel region and top-view structure of a typical CNT FET. (**B** and **C**) Transfer characteristics (B) and output characteristics (C) of the CNT FET. (**D**) Low-bias (V_{ds} = −0.1 V) linear region conductance G_{on} and peak transconductance g_m in the saturated region (V_{ds} = −1 V), showing very high on-state performance of the device. (**E**) Benchmarking of g_m versus L_g of our results with reported champion CNT FETs and conventional commercial Si PMOS transistors (*15*, *21*, *29*, *31*, *32*, *53*–*55*).

date, as the most important performance metric for FETs (*28*), the value of g_m in all fabricated FETs based on CNT arrays is usually <0.4 mS/μm (*29*), versus 0.5 mS/μm for Si CMOS FETs at a similar characteristic length. As a result, the stage delay of A-CNT ICs (consisting of FETs with a 100-nm channel length) measured with a ring oscillator (RO) was ~355 ps (*30*), which is at least one order of magnitude slower than that of similar silicon ICs or randomly oriented CNT film ICs of similar size (*15*, *16*, *31*).

Here, we report a multiple-dispersion sorting process to achieve a solution containing CNTs with a diameter distribution of 1.45 ± 0.23 nm and a semiconducting purity of >99.9999% according to a series of spectroscopy characterizations (fig. S1) and electrical measurements of 1300 FETs containing at least 2 million CNTs (figs. S2 to S4). A dimension-limited self-alignment (DLSA) procedure was developed to prepare well-aligned CNT arrays on a 4-inch (10 cm) wafer with a tunable density ranging from 100 to 200 CNTs/μm, which meets the fundamental requirements for CNTs to be useful for large-scale (but not industrial) IC fabrication as shown in Fig. 1B (*7*–*9*, *17*, *20*–*23*, *29*, *32*–*44*). The FETs and ICs based on the DLSA-processed A-CNT arrays with optimized structure and process exhibit real performance exceeding that of conventional Si CMOS transistors.

Semiconducting CNT arrays with ultrahigh purity and tunable density

In our multiple-dispersion sorting process for preparing CNTs of ultrahigh semiconducting purity (fig. S1) (*45*), raw CNTs are dispersed and sorted in toluene solvent by using conjugated PCz (poly[9-(1-octylonoyl)-9*H*-carbazole-2,7-diyl]) molecules (shown schematically in fig. S1A) (*46*). This method was previously demonstrated to provide high selectivity for semiconducting CNTs (see the absorbance spectrum of PCz-sorted CNTs in toluene solvent in fig. S1D), with diameters narrowly distributed around 1.5 nm (*46*). After washing with tetrahydrofuran, the PCz-wrapped semiconducting CNTs were then redispersed in 1,1,2-trichloroethane (fig. S1C), and these processes were repeated twice. The second and third dispersion processes were crucial for removing excess PCz molecules to provide high electrical quality and monodispersed CNTs and to prevent the formation of CNT aggregates in solution, which was important for the subsequent alignment of CNTs into arrays. During each of the repeated dispersion processes, semiconducting CNTs could be further selected and purified (see fig. S1D for the absorbance spectra of redispersed CNTs in the target solvent) to achieve an extremely high semiconducting purity of >99.9999% (after multiple dispersion) according to statistical electrical characterization of a total of 1300 wide-channel A-CNT FETs (figs. S2 to S4) (*45*). The purity of the resulting CNTs could in principle be further improved by increasing the number of dispersion processes.

We developed a DLSA procedure to assemble A-CNT arrays on a 4-inch wafer (Fig. 2, A to D). After a wafer was vertically inserted in the CNT solution, a thin layer was formed on the top surface by dropping 40 μl of 2-butene-1,4-diol ($C_4H_8O_2$) close to the wafer, and this layer quickly spread around the wafer [see (*45*) for selection criteria of the top layer ($C_4H_8O_2$) and more details on DLSA]. The possible formation of hydrogen bonds (Fig. 2A) between PCz molecules (N atoms) and $C_4H_8O_2$ (H atoms in hydroxyl) allowed the PCz-wrapped CNTs with three-dimensional random orientations in the lower solvent to randomly walk into the surface region and become confined on the two-dimensional interface between the $C_4H_8O_2$ and the 1,1,2-trichloroethane solution. As the wafer was slowly pulled out (Fig. 2C), those CNTs confined on the interface then assembled onto the wafer surface through the strong affinity of $C_4H_8O_2$ and SiO_2. CNTs were self-assembled along the contact line (horizontal orientation) between the wafer and interface by dimension-limited rotational degrees of freedom (*20*, *22*), hence the name DLSA for this process.

The CNTs in the 1,1,2-trichloroethane solution did not adhere to the surface of the Si/SiO_2 wafer (fig. S5), which is the precondition for the DLSA method to work. Unlike the previously reported floating evaporative self-assembly method (*20*, *21*), the DLSA method provided full CNT coverage across the entire substrate (Fig. 2D) because the CNTs in the lower 1,1,2-trichloroethane solvent were of sufficient quantity to serve as a continuous supply of CNTs to the interface of the binary liquid system. This solution-based DLSA procedure can be maintained in quasi-dynamic equilibrium, and the substrate withdrawal speed can thus be customized at a suitable range that depends on the interface absorption rate of CNTs. The density of the CNT array can thus be controlled through the CNT concentration in the 1,1,2-trichloroethane solution (fig. S6).

An optical image of the dip-coating mechanical apparatus for preparing A-CNT arrays on a 4-inch Si wafer with the DLSA method is shown in Fig. 2E, with the CNT coverage region marked in blue. The zoomed-in scanning electron microscopy (SEM) images (Fig. 2, F to H) of the CNT arrays show details of these arrays, in particular an excellent uniformity across hundreds of micrometers (figs. S7 to S9). The high-resolution SEM image (Fig. 2H) shows a typical CNT array (using a CNT solution concentration of 40 μg/ml) covered by a 10-nm HfO_2 thin film [grown by atomic-layer deposition (ALD)], with an optimal CNT density of ~120 CNTs/μm, or tube-to-tube separation of 8 nm (fig. S6).

The cross-sectional high-resolution transmission electron microscopy (TEM) image (Fig. 2I) revealed that the prepared CNT array remained as a monolayer, even when the array density was increased to 200 to 250 CNTs/μm (by using the highest CNT solution concentration, 60 μg/ml, in 1,1,2-trichloroethane). Monolayer formation is crucial to ensure excellent electrostatic properties for CNT-array FET applications [atomic force microscope (AFM) characterization in fig. S10 further verified the monolayer property of the CNT arrays]. Extensive characterizations confirmed that the DLSA method can produce the required monolayer CNT array with a suitable density for high-performance electronics applications, which is predicted to be in the range of 100 to 200 CNTs/μm (corresponding to a CNT spacing of 5 to 10 nm) (*2*, *3*). Detailed TEM examination of hundreds of CNTs revealed that the CNTs in the devices had a narrow diameter distribution of 1.45 ± 0.23 nm (Fig. 2J, measured by TEM), which lies well within the diameter requirement of 1.2 to 1.7 nm for realizing good ohmic contacts with relevant n- and p-type contact metals (*2*, *47*, *48*).

The polarized Raman spectra of CNTs for different incident angles δ (Fig. 2K) through rotating the optics and the Raman intensity plot in polar coordinates (Fig. 2K, inset) indicate a large intensity ratio of 45 between the maximum Raman intensity (I_{max}) and minimum Raman intensity (I_{min}). This finding shows that the alignment between CNTs in the array was excellent at 8.3° [see (*45*) for calculation details; see fig. S11 for more information on the alignment uniformity across the wafer]. According to the benchmarking of the degree of alignment (Fig. 2L), the DLSA-prepared CNT arrays showed a narrower angular distribution and a higher CNT density than other reported CNT arrays produced by different methods (*9*, *20*, *23*, *25*, *49*, *50*).

Top-gate CNT-array FETs with performance exceeding that of silicon FETs

Top-gate FETs were fabricated to explore the potential of the DLSA-prepared CNT arrays for electronics applications. Figure 3A shows a SEM image of a typical top-gate CNT FET [see (*45*) and fig. S12 for detailed fabrication process flow]. Unlike the fabrication of usual CNT thin-film FETs, cleaning the as-produced CNT arrays before device fabrication was important for DLSA-prepared CNT-array FETs. In particular, our processes included a 600°C annealing process and a yttrium oxide–based coating and decoating process (*15*, *16*, *51*). In addition, we used an asymmetrical partial gate (with a gate length as short as 100 nm; see Figs. 1A and 3A) structure to improve the current on/off ratio at high voltage bias of −1 V (*52*). The height fluctuation in our monolayer CNT array channel was small (an AFM height profile is shown in fig. S10), so an ALD-grown HfO_2 gate insulator was thinned down to 7.3 nm (with a dielectric constant of ~16.8) to provide a high gate efficiency.

Our DLSA-prepared CNT-array FETs exhibited an on-state current exceeding 1.3 mA/μm under a bias voltage of −1 V and a low bias (V_{ds} = −0.1 V) current on/off ratio greater than

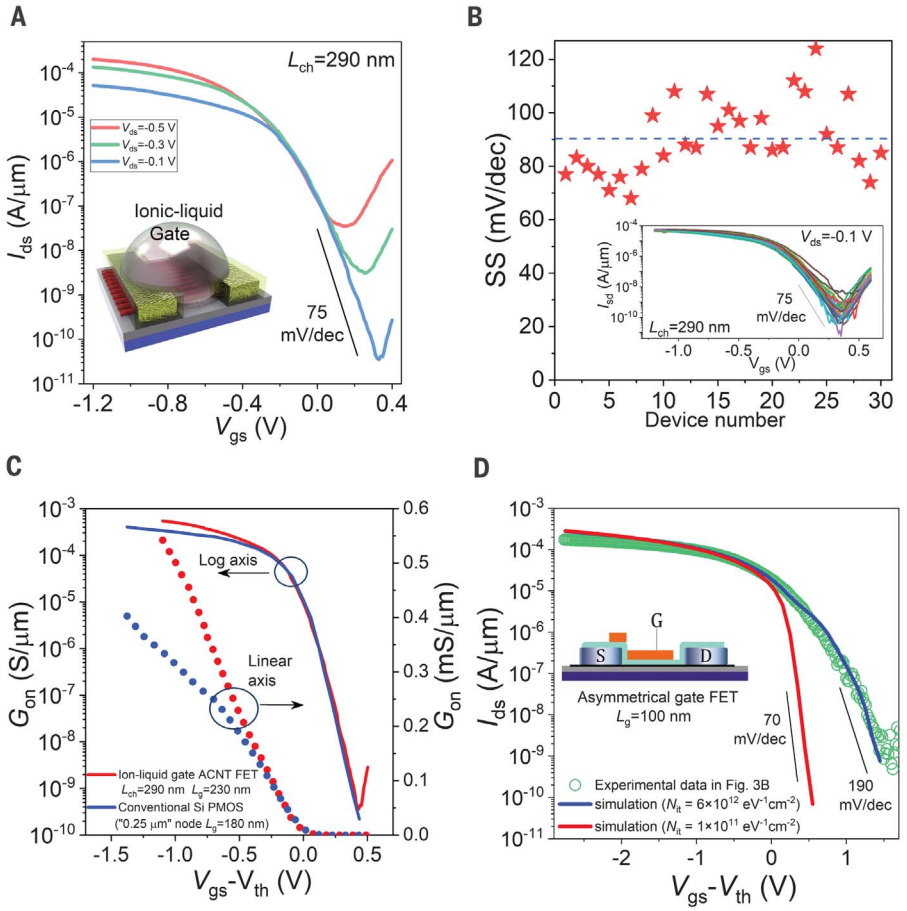

Fig. 4. Ionic-liquid gate CNT-array FETs. (**A**) Transfer characteristics of a typical FET with L_{ch} = 290 nm. Inset: Structure diagram of the ionic-liquid FET. (**B**) SS distribution of 30 ionic-liquid gate devices. Inset: Transfer characteristics of all 30 FETs. (**C**) Direct comparison of the transfer characteristics between a CNT-array FET and a Si high-performance standard PMOS FET (*54*). (**D**) Theoretically predicted transfer characteristics of CNT-array FETs with different interface state densities compared with the experimental results obtained from a top-gate CNT FET (corresponding to Fig. 3B). Inset: Device structure for both experiment and simulation.

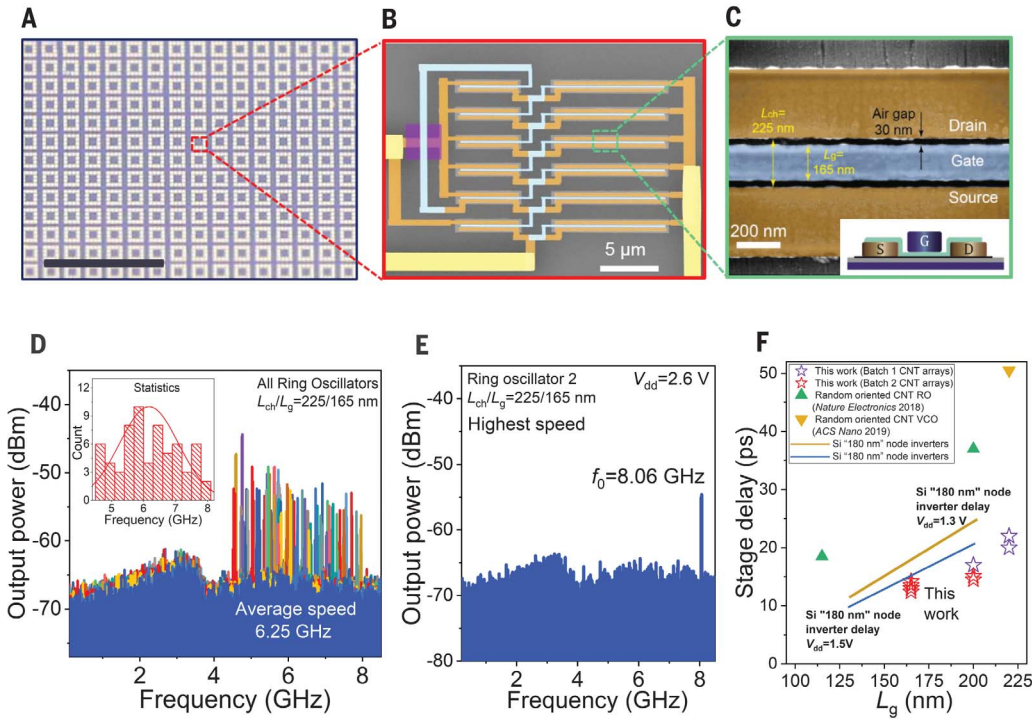

Fig. 5. Structure and characteristics of CNT five-stage ROs. (**A**) Optical image of batch-fabricated CNT five-stage ROs. Scale bar, 1.5 mm. (**B** and **C**) False-colored SEM images of a RO. The inset of (C) shows the gate structure of the CNT FET used for constructing the RO. (**D**) Power spectra of 65 CNT ROs under V_{dd} = 2.5 V; the inset shows statistical results of the switching frequency. (**E**) Power spectrum from the champion RO with the highest stage switching speed of 80.6 GHz. (**F**) Benchmarking of the stage delay of our champion ROs with state-of-the-art "0.18 μm" silicon inverters and other champion CNT ROs with similar gate lengths (*15*, *16*, *31*).

10^5 (Fig. 3, B and C). The peak transconductance g_m of the FET reached 0.9 mS/μm (at V_{ds} = −1 V; Fig. 3D), which is much higher than that of all reported CNT-based high-performance FETs (*15*, *16*, *18*, *21*, *23*–*25*, *29*, *30*, *32*). Considering that the CNT density was ~100 CNTs/μm, the peak g_m was converted to ~9 μS per CNT, which is the highest among all CNT film transistors (*15*, *16*, *18*, *21*, *23*–*25*, *29*, *30*, *32*). This value suggested that the outstanding performance of the CNT-array FET originated from contributions of all CNTs in the array, even for such a high array density. These typical CNT-array FETs exhibited higher g_m than that of Si FETs with similar gate length, including 0.13-, 0.18-, 0.25-, and 0.35-μm nodes (high-performance standards; Fig. 3E) (*31*, *53*–*55*). When benchmarked against other reported high-performance CNT-based FETs (with current on/off ratio at least two orders of magnitude) (*15*, *21*, *29*, *32*), our device showed not only much higher g_m but also lower subthreshold swing (SS) (see fig. S13). The simultaneous high g_m and low SS resulted from excellent CNT-array films with high density, good alignment, and high semiconducting purity, as well as an optimized device fabrication procedure that leads to very clean materials, excellent contacts, and a high gate efficiency for every CNT in the channel.

The SS of the top-gate CNT-array FET ranged from 100 to 200 mV/decade, which is better than that of most high-performance CNT-based FETs. However, this value still falls below the standard SS requirement (below 100 mV/decade) for digital ICs and is much higher than that based on individual CNTs with similar gate efficiency (*5*). One important factor that contributes to the SS degradation is the diameter variations of the CNTs in the arrays used in the FET channels. By a simple theoretical analysis using the virtual source model and Monte Carlo method, we found that the variation arising from the diameter distribution of our CNTs (1.45 ± 0.23 nm) would only degrade SS down to ~65 mV/decade for the top-gate CNT-array FETs (fig. S14). However, the interface-trapped charge density around the CNT channel degraded SS because these trapped charges may severely screen the electric field and lower the gate efficiency.

The effect of the interface-trapped charges on the SS of a typical FET can be discussed using the formula

$$SS = \frac{dV_g}{d(\log I_{ds})} = 2.3\frac{mkT}{q} \approx 2.3\left(1+\frac{qN_{it}}{C_g}\right)\frac{kT}{q} \quad (1)$$

(*56*), where q is the elementary charge, k is the Boltzmann constant, T is temperature, and m is referred to as the ideality factor, which is determined mainly by the interface state fixed charge density (N_{it}) and gate capacitance C_g. N_{it} is well established to be on the order of 10^{12} eV^{-1} cm^{-2} in solution-derived CNT film FETs (*56*), which is two orders of magnitude higher than that in conventional Si CMOS FETs (*57*).

This large charge density N_{it} contributes to the nonideal subthreshold performance of the CNT-array FET or large SS. Lowering N_{it} during device fabrication is difficult because it mainly results from the polymer residues wrapping the CNTs. The most effective way to improve SS would be to further improve the gate efficiency (i.e., increase C_g). We thus constructed ionic liquid (IL)–gated FETs based on the DLSA-prepared CNT arrays (Fig. 4), where the electric double layers at the IL/solid interface act as nanogap capacitors with extremely large capacitance (*58*–*60*) [see (*45*) and fig. S15 for the fabrication and measurement setup].

The adoption of an ultrahigh-efficiency IL gate improved the switching-off property of CNT-array FETs. In particular, it lowered the SS of a typical CNT-array FET to 75 mV/decade (Fig. 4A). The SS values of 30 IL-gate devices were distributed in a narrow range, with an average value of ~90 mV/decade (Fig. 4B), and the SS values of some devices even approached the 60 mV/decade theoretical limit at room temperature. A direct comparison of the transfer characteristics of an IL-gated CNT-array FET (L_{ch} = 290 nm) and those of a commercial Si PMOS (p-type metal-oxide semiconductor) FET with similar gate length (0.25-μm node with physical gate length of 0.18 μm; Fig. 4C) (*54*) showed that the CNT-array FET exhibited better on-state current and similar off-state current in a smaller V_{gs} range than that of the Si PMOS FET.

Although the IL gate is not suitable for scalable integration of solid-state devices, it

reflects the potential of CNT-array FETs with enhanced gate efficiency or lowered interface state density. Quantitative simulations revealed that if the interface state density could be lowered to 10^{11} eV^{-1} cm^{-2} (still higher than that in Si CMOS FETs), then the CNT-array FET with a solid-state gate dielectric could improve SS from 190 to 70 mV/decade (Fig. 4D and table S3) (*45*).

CNT array–based ring oscillators with a frequency of >8 GHz

Relative to a randomly oriented CNT film, an aligned CNT array with high purity and suitable density should provide better circuit performance due to notably enhanced current driving ability as well as smaller intrinsic capacitance. To demonstrate this, we used our DLSA-prepared, wafer-scale CNT arrays to construct high-performance ICs, particularly the RO circuit, which is a special standard test IC for assessing the performance and uniformity of new IC technology. We fabricated hundreds of top-gate five-stage ROs in a 5 mm × 5 mm region [see the optical image and SEM images in Fig. 5, A to C; see (*45*) and fig. S16 for the fabrication process flow] to directly test the stage propagation delay of inverters by characterizing the actual switching frequency of ROs. The top-gate structure used here was optimized to reduce parasitic capacitances between the gate and source/drain (with a 30-nm air gap on each side of the gate) and to reduce the gate resistance (tall metal gate) (*15*, *16*).

The channel and gate lengths of the CNT-array FETs used for constructing ROs were designed to be 225 and 165 nm, respectively. Typical output and transfer characteristics of the FETs are shown in fig. S17, with an on-state current of ~0.75 mA/μm and a peak g_m of >0.5 mS/μm. We measured 128 five-stage ROs in one region of the wafer (Fig. 5A), among which 65 ROs functioned successfully, indicating a yield of >50%, which is a relatively high yield among laboratory-fabricated ROs. (*15*, *30*) The frequency spectra of these ROs are shown in Fig. 5D; the corresponding oscillating frequency f_o ranged from 4.7 to 8 GHz, with an average RO switching frequency of f_o = 6.25 GHz under supply voltage V_{dd} = 2.5 V. The ROs also oscillated well (f_o = 7 GHz) under much lower V_{dd} (down to 1.8 V; see fig. S18). The highest f_o reached 8.06 GHz at V_{dd} = 2.6 V (Fig. 5E), corresponding to a stage-switching speed of 80.6 GHz and a stage delay of 12.4 ps.

We benchmarked these results with the actual speed of several representative types of IC technologies based on the measured stage delay according to different benchmarking conditions (V_{dd} or gate length L_g; Fig. 5F and fig. S18B). The DLSA-prepared CNT array–based ROs displayed lower gate delays than all reported nanomaterials-based ROs with similar gate lengths and under lower V_{dd}. In addition, our CNT array–based ICs exhibited real performance (speed) exceeding that of conventional Si CMOS ICs under similar gate lengths (Fig. 5F) (*31*).

Outlook

We showed, by combining multiple-dispersion sorting and DLSA methods, that well-aligned (within 9° of alignment), high-purity (better than 99.9999%), and high-density (tunable between 100 and 200 CNTs/μm) arrays of CNTs can be prepared on 4-inch silicon wafers with full wafer coverage; these CNT arrays meet the fundamental requirements for large-scale fabrication of digital ICs. Preliminary demonstrations using DLSA-prepared CNT arrays show that these CNT-array FETs and ICs outperform those of silicon technology with similar characteristic lengths in several key performance metrics.

Further development of this CNT-based platform will require optimization of both the material preparation and corresponding device fabrication processes. First, further improvement of the uniformity of the tube-to-tube pitch, direction, and diameter of CNTs on a large scale (such as on an 8-inch wafer) is necessary for ultralarge-scale integration of CNT ICs, particularly for sub–10 nm technology nodes. Moreover, the CNTs in the array need to be further cleaned. A certain amount of polymer residue remains wrapped around the CNTs; this prevents the formation of better contacts with smaller resistance at the source/drain and contributes to the high interface charge density (N_{it}) in the gate stack of CNT FETs (*15*, *16*, *51*). Decoupling the polymer residues from the CNT arrays while not introducing additional damage is an important issue for the fabrication of high-performance, high-reliability transistors using DLSA-prepared CNT arrays. The adoption of the multilayer interconnect technology widely used in Si technology and the optimization of the device structure would also be expected to further improve the working speed of CNT-based ICs.

REFERENCES AND NOTES

1. Semiconductor Industry Association, *2015 International Technology Roadmap for Semiconductors* (2015); www.semiconductors.org/resources/2015-international-technology-roadmap-for-semiconductors-itrs/.
2. G. S. Tulevski *et al.*, *ACS Nano* **8**, 8730–8745 (2014).
3. A. D. Franklin, *Nature* **498**, 443–444 (2013).
4. R. Chau *et al.*, *IEEE Trans. NanoTechnol.* **4**, 153–158 (2005).
5. C. Qiu *et al.*, *Science* **355**, 271–276 (2017).
6. P. Zhang *et al.*, *Nano Res.* **8**, 1005–1016 (2015).
7. Y. Hu *et al.*, *Nat. Commun.* **6**, 6099 (2015).
8. S. H. Jin *et al.*, *Nat. Nanotechnol.* **8**, 347–355 (2013).
9. J. Si *et al.*, *ACS Nano* **12**, 627–634 (2018).
10. N. Patil *et al.*, *IEEE Trans. NanoTechnol.* **10**, 744–750 (2010).
11. J. Zhang *et al.*, *IEEE Trans. Comput. Aided Des. Integrated Circ. Syst.* **31**, 453–471 (2012).
12. S. Qiu *et al.*, *Adv. Mater.* **31**, e1800750 (2019).
13. B. Chen *et al.*, *Nano Lett.* **16**, 5120–5128 (2016).
14. Y. Yang, L. Ding, J. Han, Z. Zhang, L.-M. Peng, *ACS Nano* **11**, 4124–4132 (2017).
15. D. Zhong *et al.*, *Nat. Electron.* **1**, 40–45 (2018).
16. L. Liu *et al.*, *ACS Nano* **13**, 2526–2535 (2019).
17. G. Hills *et al.*, *Nature* **572**, 595–602 (2019).
18. C. Zhao *et al.*, *Adv. Funct. Mater.* **29**, 1808574 (2019).
19. C.-S. Lee, E. Pop, A. D. Franklin, W. Haensch, H.-S. P. Wong, *IEEE Trans. Electron Dev.* **62**, 3070–3078 (2015).
20. Y. Joo, G. J. Brady, M. S. Arnold, P. Gopalan, *Langmuir* **30**, 3460–3466 (2014).
21. G. J. Brady *et al.*, *Sci. Adv.* **2**, e1601240 (2016).
22. M. Engel *et al.*, *ACS Nano* **2**, 2445–2452 (2008).
23. Q. Cao *et al.*, *Nat. Nanotechnol.* **8**, 180–186 (2013).
24. T. A. Shastry *et al.*, *Small* **9**, 45–51 (2013).
25. M. G. Zhu, J. Si, Z. Zhang, L. M. Peng, *Adv. Mater.* **30**, e1707068 (2018).
26. X. He *et al.*, *Nat. Nanotechnol.* **11**, 633–638 (2016).
27. F. Léonard, *Nanotechnology* **17**, 2381–2385 (2006).
28. S. M. Sze, K. K. Ng, *Physics of Semiconductor Devices* (Wiley, 2006).
29. Q. Cao, J. Tersoff, D. B. Farmer, Y. Zhu, S.-J. Han, *Science* **356**, 1369–1372 (2017).
30. S.-J. Han *et al.*, *Nat. Nanotechnol.* **12**, 861–865 (2017).
31. S. Yang *et al.*, in *International Electron Devices Meeting 1998. Technical Digest* (IEEE, 1998), pp. 197–200.
32. Y. Cao *et al.*, *ACS Nano* **10**, 6782–6790 (2016).
33. L. Ding *et al.*, *Nano Lett.* **9**, 800–805 (2009).
34. W. Zhou, S. Zhan, L. Ding, J. Liu, *J. Am. Chem. Soc.* **134**, 14019–14026 (2012).
35. M. M. Shulaker *et al.*, *Nature* **501**, 526–530 (2013).
36. F. Yang *et al.*, *ACS Nano* **11**, 186–193 (2017).
37. X. Xie *et al.*, *Nat. Commun.* **5**, 5332 (2014).
38. M. M. Shulaker *et al.*, in *2014 IEEE International Electron Devices Meeting* (IEEE, 2014), pp. 33.36.31–33.36.34.
39. C. Kocabas *et al.*, *Proc. Natl. Acad. Sci. U.S.A.* **105**, 1405–1409 (2008).
40. G. J. Brady *et al.*, *ACS Nano* **8**, 11614–11621 (2014).
41. Q. Cao, S. J. Han, G. S. Tulevski, *Nat. Commun.* **5**, 5071 (2014).
42. G. J. Brady, Y. Joo, S. Singha Roy, P. Gopalan, M. S. Arnold, *Appl. Phys. Lett.* **104**, 083107 (2014).
43. M. Steiner *et al.*, *Appl. Phys. Lett.* **101**, 053123 (2012).
44. Y. Cao, Y. Che, H. Gui, X. Cao, C. Zhou, *Nano Res.* **9**, 363–371 (2016).
45. See supplementary materials.
46. J. Gu *et al.*, *Small* **12**, 4993–4999 (2016).
47. W. Kim *et al.*, *Appl. Phys. Lett.* **87**, 173101 (2005).
48. Z. Chen, J. Appenzeller, J. Knoch, Y.-M. Lin, P. Avouris, *Nano Lett.* **5**, 1497–1502 (2005).
49. Z. Ma *et al.*, *Appl. Phys. Lett.* **108**, 063114 (2016).
50. S. Shekhar, P. Stokes, S. I. Khondaker, *ACS Nano* **5**, 1739–1746 (2011).
51. Z. Ma, J. Han, S. Yao, S. Wang, L.-M. Peng, *ACS Appl. Mater. Interfaces* **11**, 11736–11742 (2019).
52. C. Qiu *et al.*, *ACS Nano* **9**, 969–977 (2015).
53. S. Tyagi *et al.*, in *International Electron Devices Meeting 2000. Technical Digest* (IEEE, 2000), pp. 567–570.
54. A. Brand *et al.*, *Intel Tech. J. Q.* **3**, 1998 (1998).
55. M. Bohr *et al.*, in *Proceedings of 1994 IEEE International Electron Devices Meeting* (IEEE, 1994), pp. 273–276.
56. L. Xu, N. Gao, Z. Zhang, L.-M. Peng, *Appl. Phys. Lett.* **113**, 083105 (2018).
57. G. Kapila, B. Kaczer, A. Nackaerts, N. Collaert, G. Groeseneken, *IEEE Electron Device Lett.* **28**, 232–234 (2007).
58. M. M. Perera *et al.*, *ACS Nano* **7**, 4449–4458 (2013).
59. J. Ye *et al.*, *Proc. Natl. Acad. Sci. U.S.A.* **108**, 13002–13006 (2011).
60. J. Xia, F. Chen, J. Li, N. Tao, *Nat. Nanotechnol.* **4**, 505–509 (2009).

ACKNOWLEDGMENTS

We thank D. Zhong (Stanford University) for useful discussion, W. Liu (Peking University) for AFM technique support, and J. Yang (Peking University) for discussions on polarized Raman data. **Funding:** Supported by the National Key Research & Development Program (grants 2016YFA0201901 and 2016YFA0201902), the National Natural Science Foundation of China (grant 61888102), and the Beijing Municipal Science and Technology Commission (grant Z181100004418011). **Author contributions:** Z.Z. and L.-M.P. were in charge of and advised and led on this project; L.L. was involved in most aspects of this work, from CNT material

characterization to device/IC fabrication and device/IC characterization, and analyzed the results with Z.Z. and L.-M.P.; J.H. designed and produced dense A-CNT arrays, including the multiple dispersion process as well as the DLSA process; L.L. and J.H. characterized the A-CNT material and worked together for material system improvement; L.L., H.S., and Z.M. performed the polarized Raman spectroscopy characterization; L.X. performed the SS/N_{it} simulations based on top-gate devices using the VS model, Monte Carlo model, and TCAD; M.X. helped improve the ion-liquid device measurement; J.Z., C.Z., and H.S. were involved in device fabrication; S.D. and C.J. performed TEM experiments; L.L., Z.Z., and L.-M.P. co-wrote the manuscript. All authors commented on and discussed this work. **Competing interests:** The authors declare no competing interests. **Data and materials availability:** All data needed to evaluate the conclusions in the paper are present in the paper or the supplementary materials.

SUPPLEMENTARY MATERIALS

science.sciencemag.org/content/368/6493/850/suppl/DC1
Materials and Methods
Figs. S1 to S18
Tables S1 to S3

16 December 2019; accepted 9 April 2020
10.1126/science.aba5980

Science

Aligned, high-density semiconducting carbon nanotube arrays for high-performance electronics

Lijun Liu, Jie Han, Lin Xu, Jianshuo Zhou, Chenyi Zhao, Sujuan Ding, Huiwen Shi, Mengmeng Xiao, Li Ding, Ze Ma, Chuanhong Jin, Zhiyong Zhang and Lian-Mao Peng

Science **368** (6493), 850-856.
DOI: 10.1126/science.aba5980

Aligning dense carbon nanotube arrays

Although semiconducting carbon nanotubes (CNTs) are promising candidates to replace silicon in transistors at extremely small dimensions, their purity, density, and alignment must be improved. Liu *et al.* combined a multiple dispersion sorting process, which improves purity, and a dimension-limited self-alignment process to produce well-aligned CNT arrays on a 10-centimeter silicon wafer. The density is sufficiently high (100 to 200 CNTs per micrometer) that large-scale integrated circuits could be fabricated. With ionic liquid gating, the performance metrics exceeded those of conventional silicon transistors with similar dimensions.

Science, this issue p. 850